REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-6 remain pending in the application. Claims 1-6 are amended by the present amendment. No new matter is presented.[1]

In the Office Action, the Abstract was objected to; the Information Disclosure Statement filed June 21, 2006, was not fully acknowledged; Claims 1-6 were objected to as containing informalities; Claims 4 and 6 were rejected under 35 U.S.C. § 112, second paragraph, as indefinite; Claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as anticipated by Kutaragi et al. (U.S. Patent 5,111,530, herein "Kutaragi"); and Claims 3-6 were rejected under 35 U.S.C. § 103(a) as unpatentable over Kutaragi in view of Davis et al. (U.S. Patent 4,991,169, herein "Davis").

Regarding the objection to the Abstract, a new Abstract is submitted that conforms to M.P.E.P. § 608.01(b). Applicant respectfully requests that the objection to the Abstract be withdrawn.

Regarding the objections to Claims 1-6, Applicant has amended these claims to address the informalities noted in the Office Action. Applicant respectfully requests that the objections to Claims 1-6 be withdrawn.

Regarding the rejection of Claims 4 and 6 under 35 U.S.C. § 112, second paragraph, Applicant has amended these claims to remove the phrase "plural commands." Applicant

[1] The amendment to Claims 1 and 2 finds support in the specification at least at the paragraph bridging pages 6 and 7. The amendment to Claims 4 and 6 finds support in the specification at least at the paragraph bridging pages 42 and 43.

respectfully requests that the rejection of Claims 4 and 6 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as anticipated by Kutaragi. In response to this rejection, Applicant respectfully submits that independent Claims 1 and 2 recite novel features not taught or rendered obvious by the applied reference.

Independent Claim 1 recites, in part, a data processor, including

> a DSP configured to perform preset processing, to have at least two bus cycles in a unit of one data access, and to use a selectable number of the bus cycles in the unit of one data access; and
> an external memory configured to be accessed by the DSP and to be accessed through the DSP by the CPU, wherein
> a data word length accessed by the DSP at the external memory is variable . . . .

Turning to the applied reference, Kutaragi is directed to a digital audio signal generating apparatus for use in an electronic musical instrument. In one embodiment, Kutaragi describes a synchronizing circuit, by which a DSP and a CPU can access data at an external RAM in a time-division manner. In the Kutaragi synchronizing circuit, a time-division control circuit generates a switching control signal such that three access periods to the external RAM each have equal intervals.[2] Specifically, Kutaragi describes displacing and adjusting DSP and CPU memory accesses into equal 330 nanosecond intervals within a single machine cycle.[3]

That is, Kutaragi merely describes dividing a machine cycle into a predetermined number of equal memory access intervals. Thus, Applicant respectfully submits that

[2] Col. 16, l. 25-27, 30-45.
[3] Col. 16, l. 23-27, 30-32.

Kutaragi does not teach or suggest a DSP configured to use a ***selectable*** number of bus cycles in a unit of one data access, as recited in amended Claim 1.

Moreover, assuming *arguendo* that Kutaragi discloses that a data length to be accessed to an external memory is variable, Applicant respectfully submits that Kutaragi does not teach or suggest that a data ***word*** length accessed by a DSP at an external memory is variable, as recited in amended Claim 1.

Thus, Applicant respectfully submits that amended Claim 1 patentably distinguishes over Kutaragi.

As discussed above, Kutaragi does not teach or suggest a DSP configured to use a selectable number of bus cycles in a unit of one data access. Therefore, Kutaragi also fails to teach or suggest the DSP recited in amended Claim 2.

As additionally discussed above, Kutaragi does not teach or suggest that a data word length accessed by a DSP at an external memory is variable. Thus, Kutaragi also fails to teach or suggest the DSP recited in amended Claim 2.

Consequently, Applicant respectfully submits that amended Claim 2 patentably distinguishes over Kutaragi.

Claims 3 and 5 were rejected under 35 U.S.C. § 103(a) as unpatentable over Kutaragi in view of Davis. In response to this rejection, Applicant respectfully submits that independent Claims 3 and 5 recite novel features not taught or rendered obvious by the applied references.

Independent Claim 3 recites, in part, a data processor including an access determination unit configured to determine, when each of a plurality of DSPs issues a read

command or a write command at a same time, which one of the DSPs is allowed to access a memory.

Turning to the applied references, the Office Action appears to concede that Kutaragi does not teach or suggest the claimed access determination unit by relying on Davis to provide this feature.

Davis is directed to a system of providing information services from digital data processing centers to diversely equipped users using only digital processing equipment at the centers. The Davis system includes two processing elements, 20 and 21, to which time staggered cycling timing signals B and D are applied.[4] In Davis, signals B and D are applied so that their application in processor 20 is 180 degrees out of phase with their application in processor 21.[5] Further to Davis, signal C + D controls passing address signals from processor 20 during C and D times and from processor 21 during A and B times; processor 20 originating at signals during B times and processor 21 originating its signals during D times.[6] According to Davis, an address multiplexer is operated to initiate data accesses for processor 21 during A and B times and processor 20 during C and D times.[7] In Davis, data read out for processor 20 is latched at D times, and for processor 21 at B times.[8] Further to Davis, a write data multiplexer operates to write data from processor 21 at B and C times and from processor 20 at A and D times.[9] As shown in Davis at Figure 10, times A, B, C, and D never overlap. Thus, the times at which Davis processors 20 and 21 operate is mutually exclusive.

[4] Col. 9, l. 30-34.
[5] Col. 9, l. 33-37.
[6] Col. 9, l. 37-41.
[7] Col. 9, l. 51-54.
[8] Col. 9, l. 54-56.
[9] Col. 9, l. 57-59.

Therefore, Davis does not teach or suggest an access determination unit configured to determine, when each of a plurality of DSPs issues a read command or a write command ***at a same time***, which one of the DSPs is allowed to access a memory, as recited in amended Claim 3.

Therefore, Kutaragi and Davis, either taken alone or in combination, fail to teach or suggest an access determination unit configured to determine, when each of a plurality of DSPs issues a read command or a write command at a same time, which one of the DSPs is allowed to access a memory. Therefore, Applicant respectfully submits that amended Claim 3 (and all associated dependent claims) patentably distinguishes over any proper combination of Kutaragi and Davis.

As discussed above, the Office Action apparently concedes that Kutaragi does not teach or suggest an access determination unit configured to determine, when each of a plurality of DSPs issues a read command or a write command at a same time, which one of the DSPs is allowed to access a memory. Furthermore, as also discussed above, Davis fails to suggest such an access determination unit. Therefore, Applicant respectfully submits that no proper combination of Kutaragi and Davis teaches or suggests the access determination unit recited in amended Claim 5. Thus, Applicant further submits that amended Claim 5 (and all associated dependent claims) patentably distinguishes over any proper combination of Kutaragi and Davis.

Consequently, in view of the present amendment and in light of the foregoing comments, it is respectfully submitted that the invention defined by Claims 1-6 is definite and patentably distinguishing over the applied references. The present application is therefore believed to be in condition for formal allowance. An early and favorable reconsideration of this application is requested.

Respectfully submitted,

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